ABSTRACT OF THE DISCLOSURE:

To calculate pin-to-pin delay time, which is delay time from the input pin to the output pin of a logic block, and block-to-block delay time, which is delay time from an output pin of one block to an input pin of the next block, firstly, the pin-to-pin delay time and the block-to-block delay time are calculated with negligence in aging caused by a hot carrier effect, secondly, degradations caused by aged transistors connected to the input pin and the output pin, and lastly, the pin-to-pin delay time and block-to-block delay time are modified by the degradation rate.